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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/627,976	07/28/2003		0.00	T2147-908627	4		

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1751 Pinnacle Drive, Suite 500
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RECEIVED

MAR 15 2004

MILES & STOCKBRIDGE P.C.
TYSONS CORNER

CONFIRMATION NO. 4095

FILING RECEIPT



OC000000012092196

Date Mailed: 03/12/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Anne Kaszynski, ~~Residence Not Provided;~~
Jacques Abily, ~~Residence Not Provided;~~

Ablis, France
PLAISIR, France

Applicant: *BULL S.A., Les Clayes sous Bois, France*
Domestic Priority data as claimed by applicant

Foreign Applications: *FR02 09691, filed 7/30/2002*

If Required, Foreign Filing License Granted: 12/02/2003

Projected Publication Date: To Be Determined - pending completion of Missing Parts

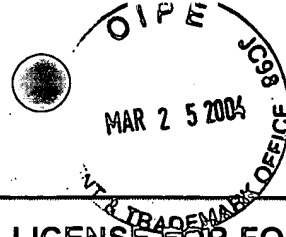
Non-Publication Request: No

Early Publication Request: No

Title

Method for functional verification of an integrated circuit model in order to create a verification platform, equipment emulator and verification platform

Preliminary Class



**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Anne KASZYNSKI & Jacques ABILY

Serial No.: 10/627,976

Filed: July 28, 2003

For: Method For Functional Verification Of An
Integrated Circuit Model For Constituting A
Verification Platform, Equipment Emulator
And Verification Platform

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: Examiner:
:
:
: Group Art Unit:
:
: Corresponding to:
: French Patent
: Application FR 02 09691

McLean, Virginia

REQUEST FOR CORRECTION OF FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Office of Initial Patent Examination's Filing Receipt Corrections

Sir:

Attached is a copy of the FILING RECEIPT – Confirmation No. 4095 in the
above-identified application mailed on March 12, 2004. We have reviewed the
accuracy of the data and request the following corrections:

In the "Applicant(s)" section, add the residence of the inventors:

--Anne Kaszynski, Ablis, France
Jacques Abily, Plaisir, France--

In the heading "Foreign Applications", add the following information:

--FR02 09691, filed 07/30/2002--

Add the following heading:

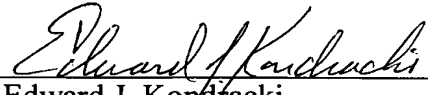
Assignee: Bull S.A., Les Clayes Sous Bois, France

Please issue a corrected Official Filing Receipt in this application.

Respectfully submitted,

MILES & STOCKBRIDGE P.C.

Date March 25, 2004

By: 
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